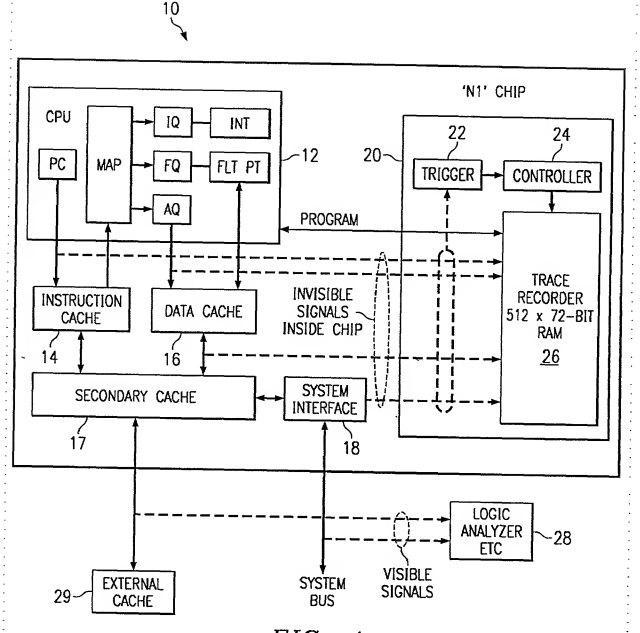

10
'N1' CHIP
CPU
PC
MAP
IQ
INT
FQ
FLT PT
AQ
12
20
22
TRIGGER
24
CONTROLLER
PROGRAM
INSTRUCTION CACHE
DATA CACHE
INVISIBLE SIGNALS INSIDE CHIP
TRACE RECORDER 512 x 72-BIT RAM
26
14
16
SECONDARY CACHE
SYSTEM INTERFACE
17
18
LOGIC ANALYZER ETC
28
29
EXTERNAL CACHE
SYSTEM BUS
VISIBLE SIGNALS

FIG. 1

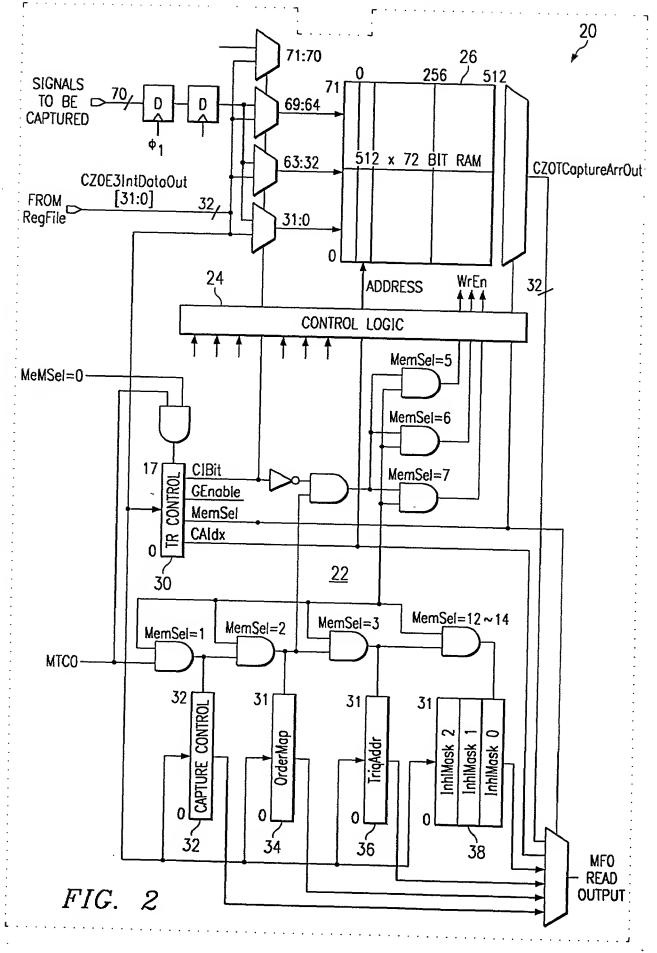
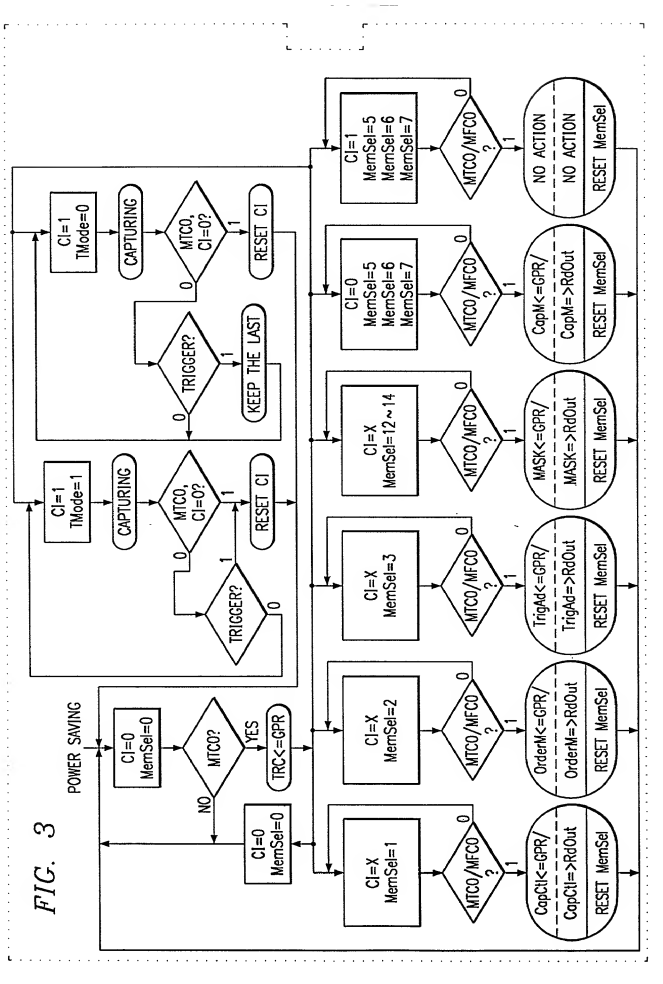

20
71:70
26
0
256
512
SIGNALS
TO BE
CAPTURED
70
D
D
ϕ_1
71
69:64
63:32
31:0
512 x 72 BIT RAM
CZ0TCaptureArrOut
CZ0E3IntDataOut
[31:0]
FROM
RegFile
32
0
24
ADDRESS
WrEn
32
CONTROL LOGIC
MeMSel=0
MemSel=5
MemSel=6
MemSel=7
17
CIBit
GEnable
MemSel
CAIdx
0
TR CONTROL
30
22
MemSel=1
MemSel=2
MemSel=3
MemSel=12~14
MTC0
32
CAPTURE CONTROL
0
32
31
OrderMap
0
34
31
TriqAddr
0
36
31
InhiMask 2
InhiMask 1
InhiMask 0
0
38
MF0
READ
OUTPUT

FIG. 2

FIG. 3



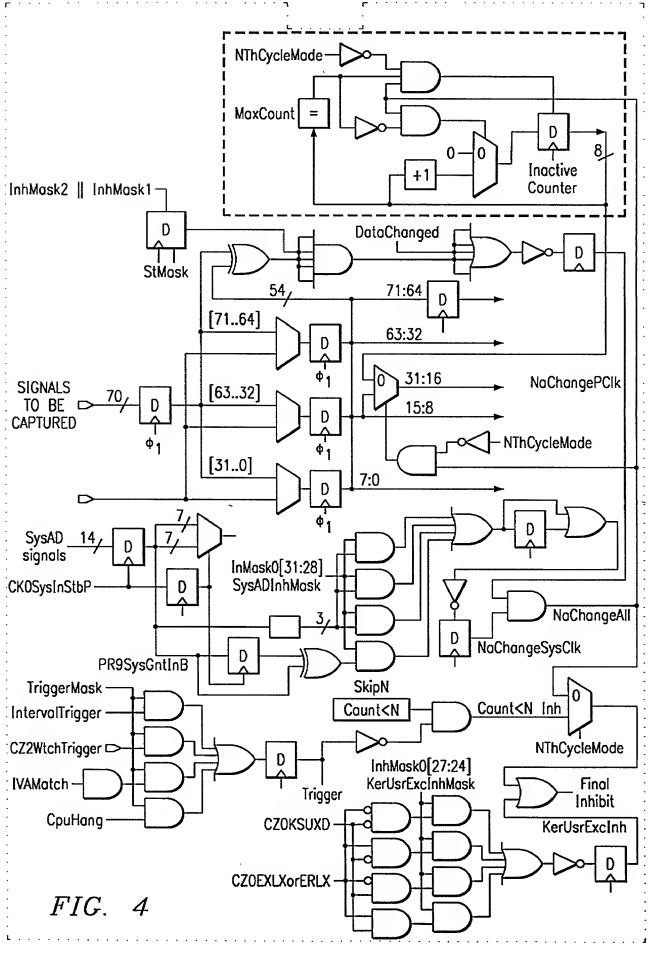

NThCycleMode
MaxCount
=
0
+1
D
Inactive Counter
8
InhMask2 || InhMask1
StMask
DataChanged
54
71:64
[71..64]
63:32
SIGNALS TO BE CAPTURED
70
[63..32]
31:16
15:8
NaChangePClk
NThCycleMode
[31..0]
7:0
SysAD signals
14
CK0SysInStbP
InMask0[31:28]
SysADInhMask
NaChangeAll
NaChangeSysClk
PR9SysGntInB
TriggerMask
IntervalTrigger
CZ2WtchTrigger
IVAMatch
CpuHang
SkipN
Count<N
Count<N Inh
NThCycleMode
Trigger
InhMask0[27:24]
KerUsrExcInhMask
Final Inhibit
KerUsrExcInh
CZ0KSUXD
CZ0EXLXorERLX

FIG. 4

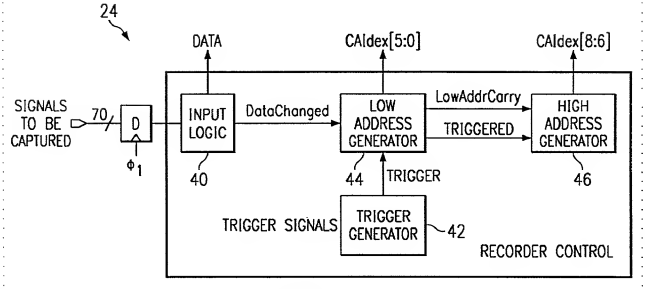

24
DATA
CAIdex[5:0]
CAIdex[8:6]
SIGNALS TO BE CAPTURED
70
D
ϕ_1
INPUT LOGIC
40
DataChanged
LOW ADDRESS GENERATOR
44
LowAddrCarry
TRIGGERED
HIGH ADDRESS GENERATOR
46
TRIGGER
TRIGGER SIGNALS
TRIGGER GENERATOR
42
RECORDER CONTROL

FIG. 5

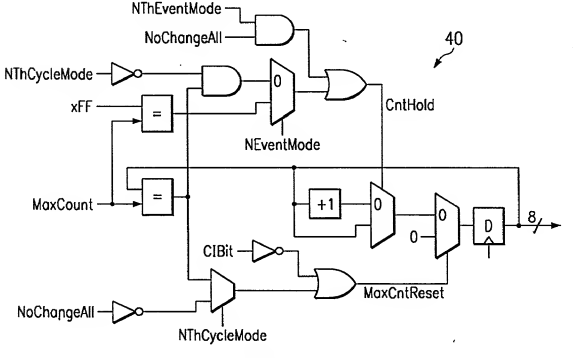

NThEventMode
NoChangeAll
40
NThCycleMode
xFF
=
0
CntHold
NEventMode
MaxCount
=
+1
0
0
0
D
8
CIBit
MaxCntReset
NoChangeAll
NThCycleMode

FIG. 6

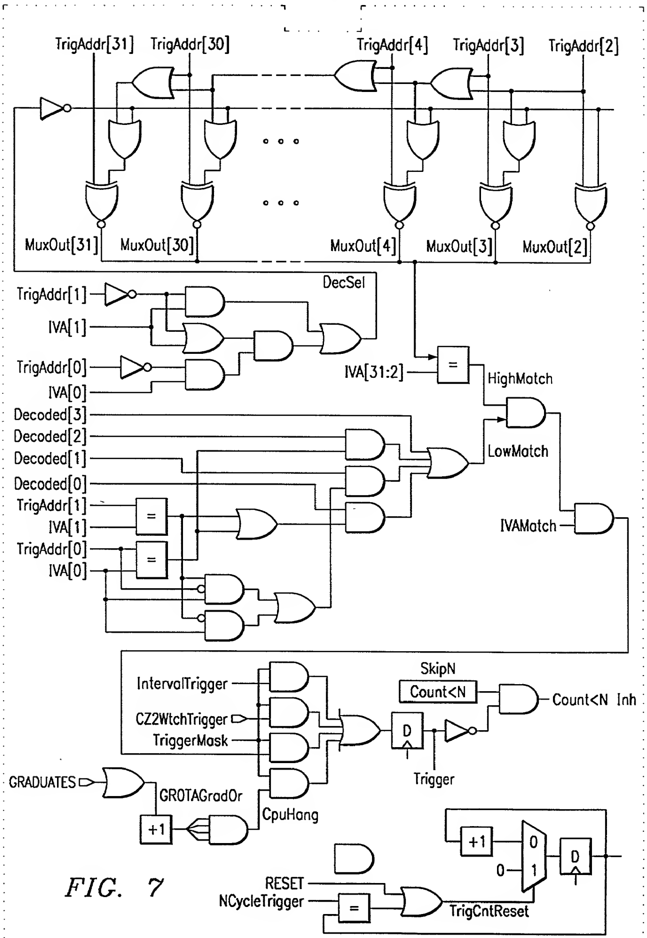


FIG. 7

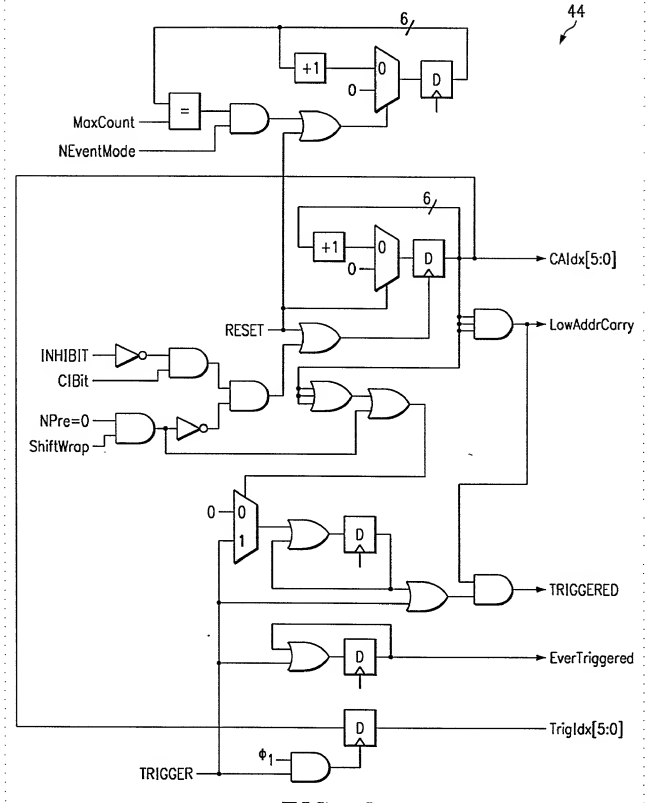

44
6
+1
0
D
=
MaxCount
NEventMode
CAIdx[5:0]
RESET
LowAddrCarry
INHIBIT
CIBit
NPre=0
ShiftWrap
TRIGGERED
EverTriggered
TrigIdx[5:0]
TRIGGER
ϕ_1

FIG. 8

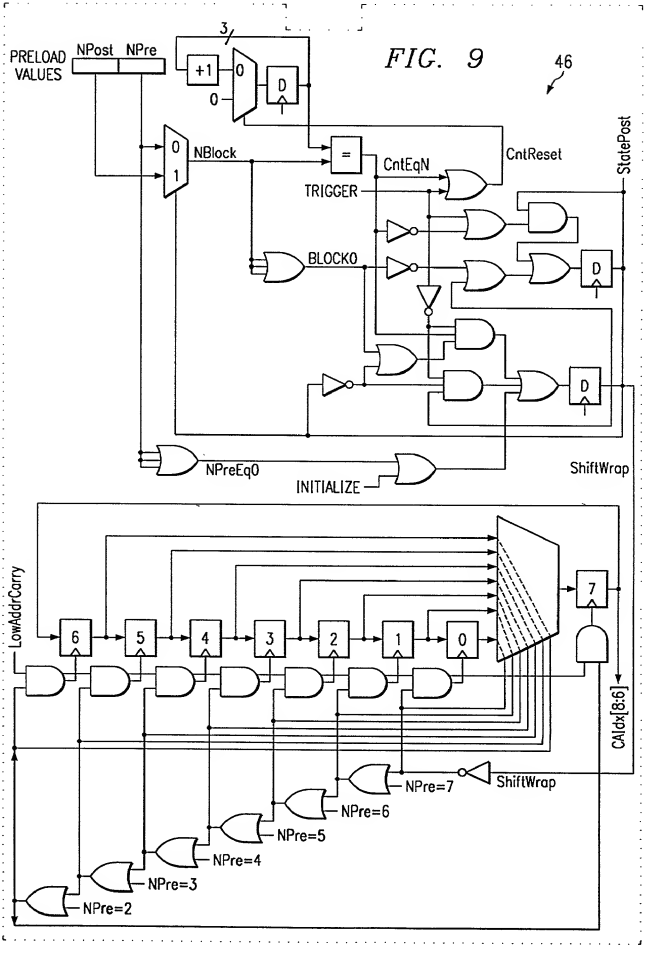

PRELOAD VALUES
NPost
NPre
3
+1
0
D
0
NBlock
=
CntEqN
CntReset
StatePost
TRIGGER
BLOCK0
D
D
NPreEq0
INITIALIZE
ShiftWrap
LowAddrCarry
6
5
4
3
2
1
0
7
CAIdx[8:6]
NPre=7
ShiftWrap
NPre=6
NPre=5
NPre=4
NPre=3
NPre=2

FIG. 9

46

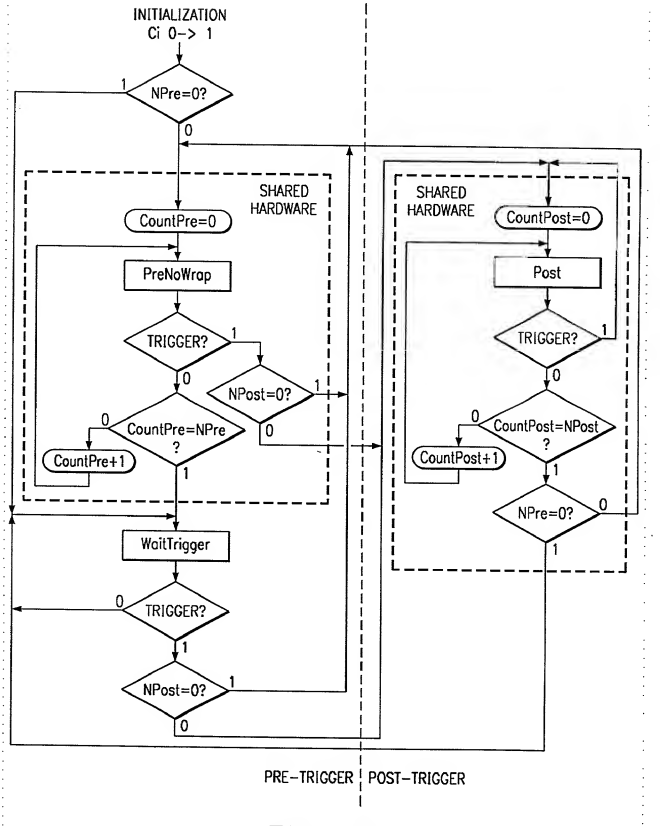

INITIALIZATION
Ci 0-> 1
NPre=0?
1
0
SHARED HARDWARE
CountPre=0
PreNoWrap
TRIGGER?
1
0
NPost=0?
1
0
CountPre=NPre ?
0
CountPre+1
1
WaitTrigger
TRIGGER?
0
1
NPost=0?
1
0
SHARED HARDWARE
CountPost=0
Post
TRIGGER?
1
0
CountPost=NPost ?
0
CountPost+1
1
NPre=0?
0
1
PRE-TRIGGER
POST-TRIGGER

FIG. 10